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RF Variable-Gain Amplifiers and AGC Loops for Digital TV Receivers

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SUMMARY RF Variable Gain Amplifiers (RF-VGA) are important components for integrated TV broadcast receivers. Analog and digital controlled RF-VGAs are compared in terms of linearity and an AGC loop architecture suitable for digitally controlled RF-VGA is proposed. Further linearity enhancement applicable for CMOS implementation is also discussed.

key words: *VGA, AGC, SiGe BiCMOS, CMOS, tuner, IIP3, linearity*

1. Introduction

Although the demand for integrated TV receiver ICs is high, they haven't been as much established as those for cellular phone or WLAN. The major factor which makes TV receiver integration difficult is the fact that TV receiver does not always receive the signal from the nearest base station but it often has to receive the signal from a far station among the stronger blocker signals from nearer stations. To cope with this situation, each TV broadcast standard imposes stringent linearity and selectivity test patterns on the receiver [1]–[4]. Some examples of these test patterns for DVB-H, a digital TV standard for mobile receivers in Europe, are shown in Table 1. In addition to them, the receiver should receive input signals of widely varying power, such as from less than −80 dBm to more than −20 dBm depending on the distance from the broadcast antenna.

To cope with these demands and expand their receiving range as much as possible, the integrated TV receiver should have an RF variable gain amplifier as the first stage of the receiver circuit. A typical tuner IC block diagram [5] is depicted in Fig. 1, where AGC loop maximizes the RF-VGA gain under the condition that the total RF-VGA output power including desired and blocker signals does not exceed a threshold level. The threshold level is predefined so that the distortions generated in the RF-VGA and the mixer are kept at allowable level. Thus the AGC assumes the RF-VGA characteristic that reduced RF-VGA gain reduces the distortion through the improved linearity. Thus the RF-VGA should be carefully designed so that it has this property. Some admissible combinations of the target specifications of the RF-VGA and the mixer are depicted in Table 2 [4]. In addition to satisfy these specifications, the RF-VGA is expected to change its NF and IIP3 monotonically along with its gain to maximize its receiving area.

Conventional "Can type tuner" uses a dual-gate FET as a VGA controlling its gain with an analog control voltage on one gate. The first RF-VGA we have developed for ISDB-Tss [5], Japanese digital TV standard for mobile receivers,

Table 1 Test patterns for DVB-H.

Pattern	Modulation of interferer	Interferer location (N: desired signal ch.)	U/D (dB)	U (dBm)
L1	digital and analog	N+2 (digital) N+4 (analog)	45	-35
L2	analog	N+2, N+4	45	-35
L3	digital	N+2, N+4	40	-35
S1	analog	N±1	38	-35
		N±k (k≠0, 1)	48	-28
S2	digital	N±1	29	-35
		N±k (k≠0, 1)	40	-28

Desired channel modulation: 16QAM
U: interferer power (on each channel)
D: desired signal power

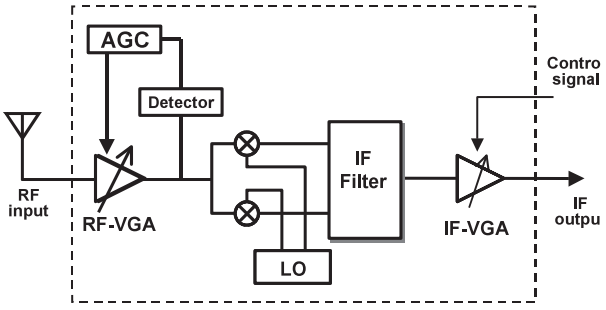

Fig. 1 Typical tuner IC block diagram.

Table 2 An example of admissible performance combination for DVB-H receiver.

	VG-LNA	Mixer	Cascaded
Max gain	Gain = 23 dB NF = 3dB IIP3 = 97 dBμV	Gain = 8 dB NF = 21 dB IIP3 = 120 dBμV	Gain = 31 dB NF = 4.2 dB IIP3 = 94 dBμV
L3	Gain = 15 dB NF = 11 dB IIP3 = 102 dBμV	Gain = 8 dB NF = 21 dB IIP3 = 120 dBμV	Gain = 23 dB NF = 12.2 dB IIP3 = 100.2 dBμV

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also has an analog control. However, we found that a digital gain control with discrete gain levels is more amenable to reduce linearity degradation. The amplitude discontinuities less than a few dB introduced by the digital gain control into the received TV signal are usually not harmful for digital signal demodulation since digital TV demodulators use pilot signals to calibrate the signal power and also employ various error corrections. (On the other hand, the discontinuities are harmful to analog TV broadcast receivers, since the analog TV broadcast uses amplitude modulation for picture brightness. We have confirmed that the discontinuities smaller than 1 dB do not have perceivable effects in analog TV.)

Section 2 reviews two RF-VGAs implemented in SiGe BiCMOS. First one is an analog control RF-VGA designed for ISDB-Tss application and the second one is a digital control RF-VGA designed for DVB-H application. In Sect. 3, a new technique to further improve the linearity of RF-VGA using CMOS transconductance is proposed. Section 4 introduces an AGC loop architecture suitable for digital control RF-VGA's and the paper is summarized in Sect. 5.

2. RF-VGA with Passive Step-Attenuators

2.1 Effects of gm Control

TV receivers require more than 60 dB variable gain range while keeping the maximum possible linearity throughout the whole gain range. Realizing the RF-VGA only with active gain stages tend to degrade the linearity. On the other hand, passive attenuators can achieve as much reduction as required without degrading the linearity. Thus we had come up with the idea of combining passive step-attenuators with active gain stages. As explained in Sect. 1, the gain should be controlled continuously or discretely with a step size of less than a few dB even for digital TV broadcast receivers.

The first RF-VGA we have designed in a SiGe BiCMOS process has a structure as in Fig. 2 [5]. It consists of three stages of step-attenuators each with 26.6 dB attenuation and four cascode common-emitter amplifiers with a combined output. The base-currents of four cascode amplifiers are controlled by a bias generator shown in Fig. 3. According as the control voltage changes, the bias currents for four amplifiers change smoothly from one to next one as in the inset of Fig. 3. Consequently, the gain of the RF-VGA continuously changes as the analog control voltage changes continuously.

The main improvement in the RF-VGA is a way to control the bias currents of the cascode amplifiers. The circuit with nested differential pairs shown in Fig. 3 is used to distribute a fixed amount of current to the common-emitter transistor bases with an appropriate ratio corresponding to the control voltage as shown in the inset of Fig. 3. Since the total current is independent of the control voltage, the DC output level is kept constant. The circuit is simpler and more power-efficient than that proposed in [6], which needs many current sources and sinks.

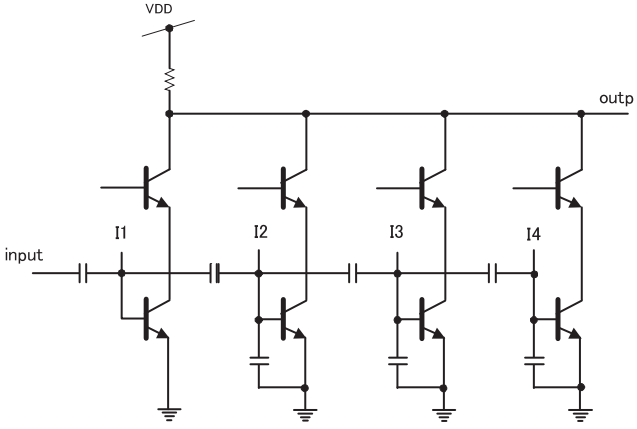


Fig. 2 RF-VGA with analog control.

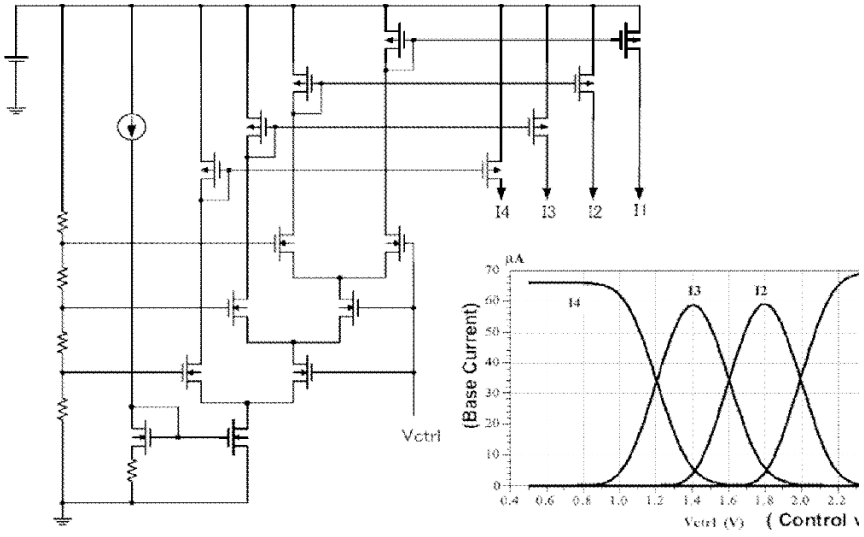


Fig. 3 Bias current generator and its output.

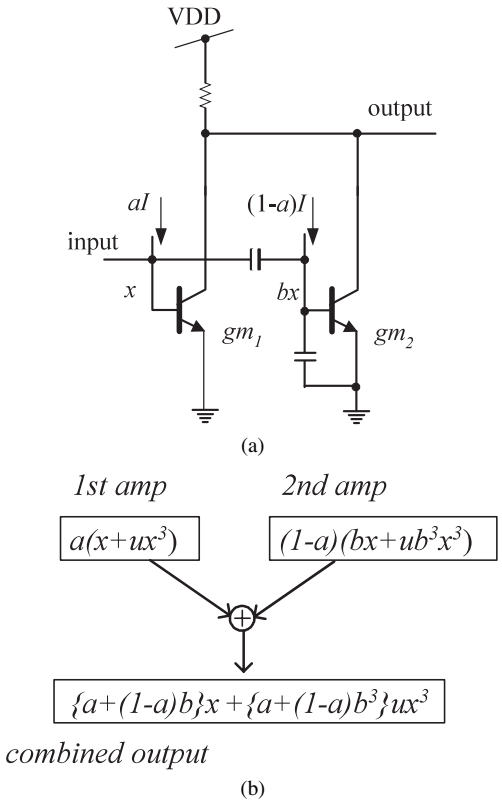


Fig. 4 (a) Schematics of first two stages of analog control RF-VGA, (b) combined output function.

For a bipolar transistor, $gm = I/Vt$, where $Vt = kT/q$ in which k is the Boltzmann constant, q the charge of an electron, and T is the absolute temperature. If the current I is divided into aI and $(1 - a)I$ for two gm stages as in Fig. 4, $gm_1 = aI/Vt$ and $gm_2 = (1 - a)I/Vt$. Therefore if the attenuation by a capacitive attenuator is b $(0 < b < 1)$, then the combined transconductance is

$$gm_1 + bgm_2 = aI/Vt + b(1-a)I/Vt = I(a+b-ab)/Vt.$$

This changes from I/Vt to bI/Vt as a decreases from 1 to 0.

Assume that the transfer function of the common-emitter stage is expressed as $a(x + ux^3)$. If the IIP3 voltage x_0 of the common-emitter stage is independent of the bias current, then the IIP3 voltage of the combined amplifier can be written as cx_0 where c is obtained from the combined output function in Fig. 4(b) as

$$cx_0 = \sqrt{\frac{4\{a + b\,(1 - a)\}}{3\{a + b^3\,(1 - a)\}u}} = \sqrt{\frac{a + b\,(1 - a)}{a + b^3\,(1 - a)}}x_0$$

since $u = \frac{4}{3x_0^2}$.

Thus IIP3 increases from x_0 to x_0/b as the base bias current I is steered from the first stage to the second stage. However, real bipolar transistors give a different result. The measurement result is shown in Fig. 5, where the measured and simulated gain and IIP3 are plotted for the control voltages from 1.75 V to 2.5 V. It is observed that the IIP3 does not monotonically increases as the gain decreases. The discrepancy tells that the assumption that the IIP3 of the bipolar gm stage is independent of the bias current is not valid.

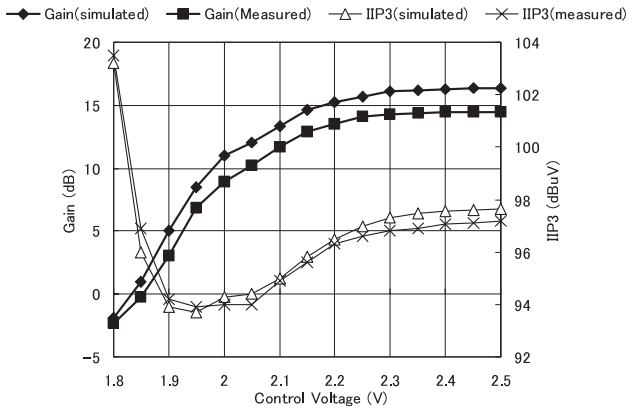


Fig. 5 Simulated gain and IIP3 vs. control voltage.

Basically, linearity of bipolar transistors is dominated by the nonlinearity of exponential function and the voltage dependence of base-collector parasitic capacitance [7], [8]. In ideal, since $I = I_0 \exp(Vbe/Vt)$ and $gm = I/Vt$, IIP3 = $2\sqrt{2}Vt = 94\,\mathrm{dB}\mu\mathrm{V}$, [9]–[11]. However, if the base-emitter current I is large, due to the feedback by emitter resistance, linearity can be increased [7]. The transconductance and the IIP3 of a bipolar transistor with parasitic emitter resistance R_e are calculated using the analysis in [9], [10] as

$$Gm = \frac{gm}{1 + R_e gm}$$

$$IIP3 = \sqrt{\frac{4 \cdot (I_c \cdot R_e)^3}{V_T}}.$$

With the measured corrector current of 6.7 mA, the emitter resistance extracted from the transistor model of 7 Ω and the load resistance of 100 Ω, the gain and IIP3 are calculated as 19.3 dB and 99 dBμV. These values reasonably agree with the measured and simulated maximum gain and IIP3 observed in Fig. 5.

2.2 Constant Current Density gm

To tackle the problem of linearity degradation of abovementioned analog control VGA for intermediate gain between two step attenuators, we introduced current steering type gain control [12], [13]. Figure 6 shows the proposed current steering VGA. The current signal generated from a gm transistor is split into two paths, a signal path and a dumping path. The gain of this VGA is controlled by n-pair of transistors which steer the current into one of two paths. The base current of gm transistor is kept constant, therefore ensuring constant linearity for any gain setting.

Replacing the cascode amplifiers in Fig. 2 by the VGAs in Fig. 6, fine-gain tuning with constant IIP3 between consecutive step attenuator outputs can be obtained [14]–[16]. Figure 7 and Fig. 8 show the measured and simulated IIP3

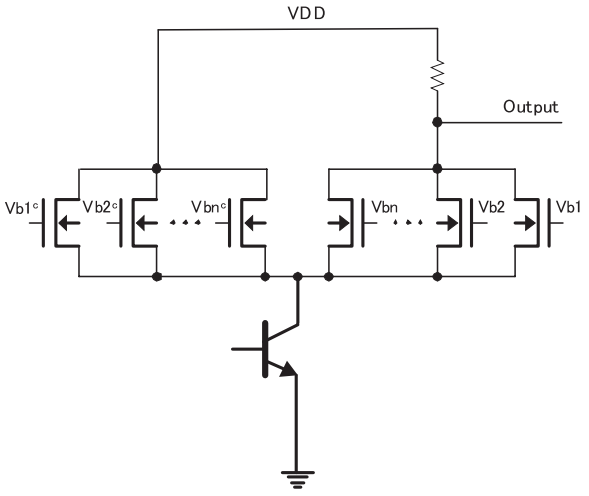


Fig. 6 Current steering type VGA.

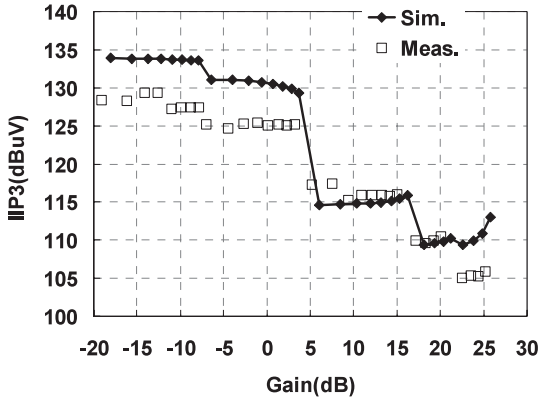


Fig. 7 Measured and simulated IIP3 vs. gain.

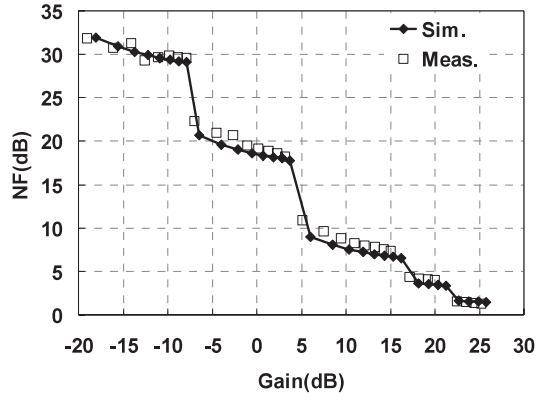


Fig. 8 Simulated NF vs. gain.

and NF of the proposed current-steering RF-VGA at 650-MHz input frequency. It is observed in Fig. 7 that IIP3 stays constant until another attenuation step is chosen as a result of current-steering type control. In addition, IIP3 itself shows better value comparing with Fig. 5. The linearization technique described in [4], which compensates the gain compression for large input signal, contributes to this improvement.

3. Current Density Control

The proposed current-steering RF-VGA in the previous section keeps IIP3 while the current is steered to the next stage to reduce the gain. In this section, a circuit for further linearity improvement is proposed with the use of CMOS for transconductor stages. The drain current of CMOS transistor is given by the equation

$$I = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{gs} - V_{th}\right)^{\alpha}, \tag{1}$$

where μ, C_{ox}, W, L, V_{gs}, and V_{th} are the mobility of the charge carriers, the gate oxide capacitance per unit area, the gate width, the gate length, the gate-source voltage, and the threshold voltage, respectively. The process-dependent parameter α is smaller than 2 in sub-micron CMOS processes [17]. For example, the NMOS transistors in a 0.18-μm CMOS process used for this study takes 1.23 as α. Taking derivative of (1), we have

$$\begin{aligned} gm &= \frac{1}{2}\alpha\mu C_{ox}\frac{W}{L}\left(V_{gs} - V_{th}\right)^{\alpha-1} \\ &= \frac{1}{2}\alpha\left(\mu C_{ox}W/L\right)^{\frac{1}{\alpha}} I^{\frac{\alpha-1}{\alpha}}, \\ gm' &= \frac{1}{2}\alpha\left(\alpha-1\right)\mu C_{ox}\frac{W}{L}\left(V_{gs} - V_{th}\right)^{\alpha-2}, \end{aligned}$$

and

$$gm'' = \frac{1}{2}\,\alpha\left(\alpha-1\right)\,\left(\alpha-2\right)\mu C_{ox}\frac{W}{L}\left(V_{gs} - V_{th}\right)^{\alpha-3}.$$

Then the voltage gain G, $IIP3$, and $OIP3$ are given by the following equations [11]:

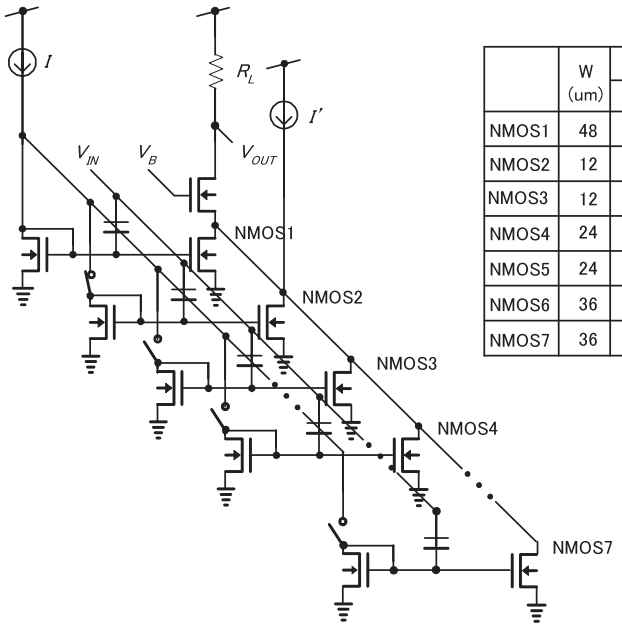
$$G = \alpha\left(\frac{1}{2}\mu C_{ox}W/L\right)^{\frac{1}{\alpha}} I^{\frac{\alpha-1}{\alpha}} R_L, \tag{2}$$

$$\begin{aligned} IIP3 &= \sqrt{\frac{4gm}{3gm''}} = \sqrt{\frac{4}{3\left(\alpha-1\right)\left(2-\alpha\right)}}\left(V_{gs} - V_{th}\right) \\ &= \sqrt{\frac{4}{3\left(\alpha-1\right)\left(2-\alpha\right)}}\left(\frac{2I}{\mu C_{ox}W/L}\right)^{\frac{1}{\alpha}}, \end{aligned}$$

and

$$OIP3 = \alpha\sqrt{\frac{4}{3\left(\alpha-1\right)\left(2-\alpha\right)}}IR_L, \tag{3}$$

where R_L is the load resistance. Thus, if we can somehow reduce W while keeping the current I constant, G decreases and IIP3 increases so that OIP3 keeps a constant value. The reduction of W is impossible in integrated circuits. However, the equivalent effect is realized with the configuration of Fig. 9. In this configuration, the number of transistors which share the fixed current I is altered. Then the off transistors do not contribute the transconductance and thus effectively the combined transistor reduces its W.



Switch Setting

	W (um)	max ← gain → min						
		1	2	3	4	5	6	7
NMOS1	48	on	on	on	on	on	on	on
NMOS2	12	on	on	on	on	on	on	off
NMOS3	12	on	on	on	on	on	off	off
NMOS4	24	on	on	on	on	off	off	off
NMOS5	24	on	on	on	off	off	off	off
NMOS6	36	on	on	off	off	off	off	off
NMOS7	36	on	off	off	off	off	off	off

Fig. 9 Current density controlled gm stage.

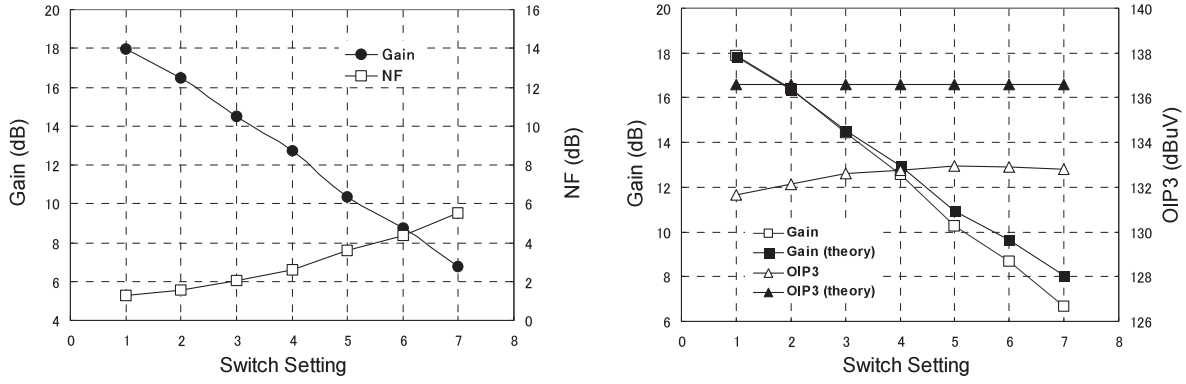


Fig. 10 Simulated performances of the proposed CMOS VGA at 868 MHz; (left) NF vs. gain and (right) OIP3 vs. gain (including theoretical values).

Simulated results by HSPICE of the gm stage at 868 MHz are shown in Fig. 10 together with the theoretical gain and OIP3 calculated by (2) and (3). The gate width of input transistors MOS1 to MOS7 are chosen to be 48, 12, 12, 24, 24, 36, and 36 μm, while the length is 0.18 μm for all the input transistors. For the minimum gain only MOS1 is ON and to increase the gain MOS2 to MOS7 are turned on in this order as described in the inset of Fig. 9. About 4 to 5 dB differences between the simulated and calculated OIP3 values arise from the non-linearity of the output impedance, which is not included in the simple model (1). However, the flatness of OIP3 is well maintained in the simulation result.

This gm stage draws 20 mA from 1.8-V supply voltage. As the Eq. (3) predicts, OIP3 is proportional to the current. Thus further reduction of the current while keeping OIP3 would require another linearization technique.

Combining the proposed gm stages with passive step attenuators, we can design an RF-VGA with more than 60-dB variable range whose IIP3 monotonically increases as the gain reduces. The silicon implementation of this RF-VGA and measurement results will be presented in a subsequent paper.

4. AGC Loop for Digitally Controlled VGA

As described in Sects. 3 and 4, the VGA with digital gain control can have better linearity than analog controlled ones. Though we designed the VGA so that it's linearity increases as the gain reduces, it performs to the best of its potential only when controlled with a decent AGC. This section introduces a new AGC loop which was designed to be used together with a VGA having digital control. The AGC architecture is described in Fig. 11, where Detector (Gilbert cell used as a multiplier) measures the instantaneous signal power of the RF-VGA output. Detector output is compared with the limit setting value and integrated with an analog

integrator. Then a successive approximation ADC designed for gain control converts the integrated analog signal into 5-bit digital control values for VGA control. The ADC has the following features:

- It has a hysteresis characteristic to avoid the fluctuation of the output.
- It changes at most 1 LSB among two consecutive samplings.

These features are realized by the structure shown in Fig. 12 as described below:

- The analog input Vin is sampled by clk1 together with the offsets of the inverters.
- While clk3 is high, the sampled input is compared by the latched comparator CMP with the output of the 6-bit R-2R D/A converter DAC-A controlled by a 6-bit counter CNT-A which plays as a SAR register.
- If the comparator output latched by clk4 is high (resp. low), both CNT-A and CNT-B down-count (resp. up-count) 1 bit. Thus at each sampling the output of DAC-A changes 1 LSB.
- If the output of CNT-B becomes 2 (resp. -2), then the 5-bit counter CNT-C, which serves as the output register of the ADC, up-count (resp. down-count) 1 bit and CNT-B is reset to zero.
- Since CNT-B is reset when CNT-C changes, it needs two up-counts or down-counts for the next change of the output. Thus the CNT-C output shows hysteresis property as in Fig. 13.

The ADC is designed to operate with the sampling frequency between 1 kHz and 100 kHz. Since only 1 LSB changes at each sampling, the effective bandwidth of this ADC is much smaller than the sampling clock. The simulation result of the ADC is shown in Fig. 14, where the digital output follows the input signal with a 1-LSB step without responding to the rapid input fluctuation. This property to-

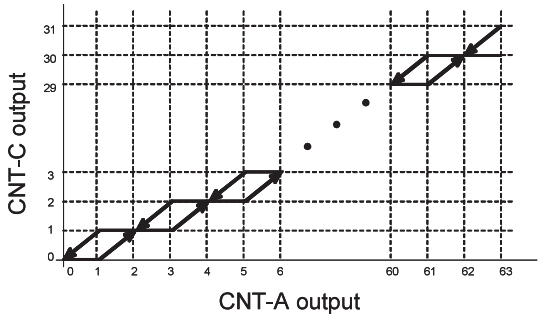


Fig. 13 Hysteresis behavior of the proposed ADC output.

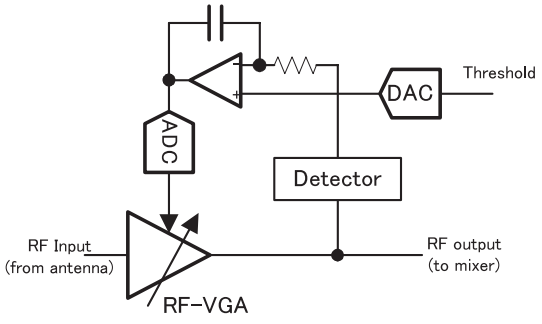


Fig. 11 AGC loop for RF-VGA with digital gain control.

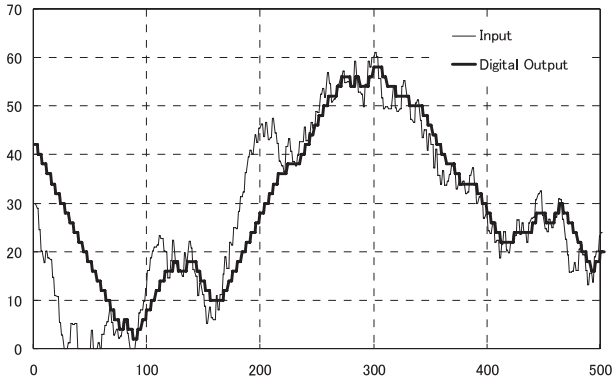


Fig. 14 Simulation result of proposed ADC.

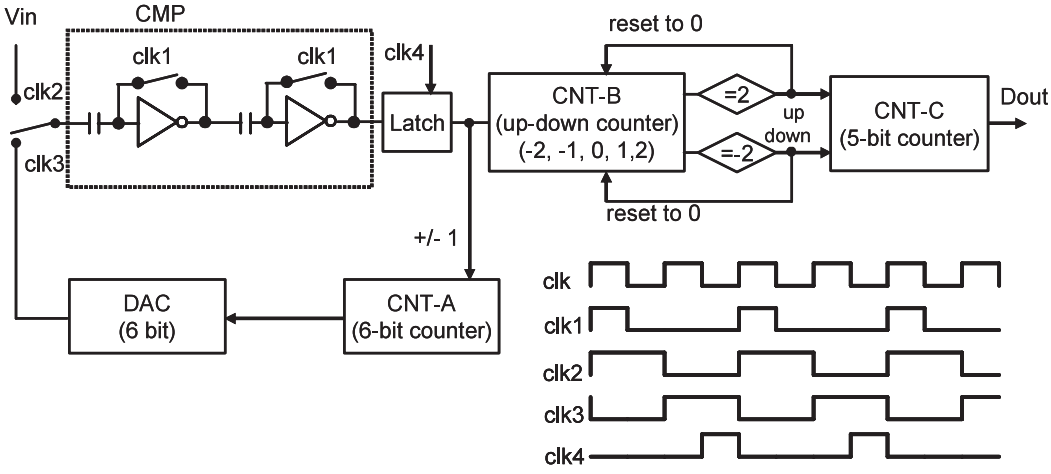


Fig. 12 Proposed ADC for an RF-VGA with digital gain control.

gether with a fine step VGA guarantees sufficiently small gain discontinuities. The effectiveness of this AGC architecture is confirmed in the DVB-H tuner IC described in [4].

5. Conclusion

In this paper, three types of RF-VGA topologies were studied. Starting from an analog control VGA, a digital control one was introduced together with a suitable AGC architecture. Then further linearity enhancement idea for CMOS VGA was proposed with simulation. Future works would include silicon implementation of the proposed CMOS VGA and the input impedance matching for wide gain range VGA's as well.

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